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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/572,981	03/21/2006	Franciscus Adrianus Schoofs	NL03 1162 US1	7644
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NXP, B.V. NXP INTELLECTUAL PROPERTY & LICENSING M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			EXAMINER TRAN, NGUYEN	
			ART UNIT 2838	PAPER NUMBER
			NOTIFICATION DATE 08/27/2009	DELIVERY MODE ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

### Office Action Summary

**Application No.**

10/572,981

**Applicant(s)**

SCHOOF ET AL.

**Examiner**

NGUYEN TRAN

**Art Unit**

2838

**Period for Reply** -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 23 October 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-22 and 24-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 3-12 is/are allowed.
- 6) ☒ Claim(s) 1,2,13-18,20,21 and 24-26 is/are rejected.
- 7) ☒ Claim(s) 19 and 22 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB08)
- Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

Claims 1-2, 13-18; 20-21, 24, and 26 are pending; claims 3-12 are allowed; claims 19 and 22 would be allowable if rewritten in independent form.

### *Response to Arguments*

Applicant's arguments filed 05/05/09 have been fully considered but they are not persuasive. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a zero load voltage (e.g., the voltage the converter should supply at zero load as is discussed in paragraphs 0004 and 0008 of Applicant's specification)) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). In addition, the Examiner fails to see how the zero load voltage is recited in claim 1 different from the voltage between the resistor 24 and the capacitor 25 of '129. In **figure 4, Col. 5, lines 40-50** teaches a differential amplifier 26 having a non-inverting input receives a voltage generated between the resistor 24 and a capacitor 25 and a inverting input receives a the voltage across the capacitor 25 corresponds to the voltage across the DC resistor of the output inductor 23. Since amplifier 26 is a differential amplifier, one with ordinary skill in the art would recognize that the differential amplifier 26 output a difference signal at the output.

In addition, Applicant argues that '129 reference does not correspond to aspects of the claimed invention directed to a switch controller for receiving the difference signal,

the momentary information and the correction signal to control the switch for obtaining a substantially zero correction signal in a steady state. The Examiner disagrees, because Emphasis added, the transitional term **"comprising"**, which is synonymous with "including," "containing," or "characterized by," is inclusive or open-ended and does not exclude additional, unrecited elements or method steps. Furthermore, **"comprising"** is a term of art used in claim language which means that the named elements are essential, but other elements may be added and still form a construct within the scope of the claim (see *Genentech, Inc. v. Chiron Corp.*, 112 F.3d 495, 501, 42 USPQ2d 1608, 1613 (Fed. Cir. 1997). Therefore, '129 teaches a switch controller **27** for receiving the difference signal (**output of 26**) the momentary information (**output of 17**) and the correction signal (**output of fig. 2**) to control the switch **21, 31** for obtaining a substantially zero correction signal in a steady state (**Col. 5 lines 64 through Col 6, lines 1-42 and Col. 7, lines 1-20**) (i.e. the switch controller **27** receiving the difference signal, the momentary information and the correction signal that outputted by the differential amplifier **26**, the differential amplifier **17** and the current sense **28** directly or indirectly through the current sense **28** to provide a signal to the PWM controller **27** in order to control the switching device **21** and **22** for obtaining a substantially zero correction signal at the output of the DC-DC voltage converter in a steady state). In addition, the Examiner fails to see how the switch controller for receiving the difference, the momentary information and the correction signal to control the switch for obtaining a substantially zero correction signal in a steady state are recited in claim 1

different from the signals provided to the PWM controller 27 through out the circuit components in order to control the switches 21 and 22 in figure 4 of '129.

Furthermore, Applicant argues that '129 reference teaches away from combining redundant circuitry from alternative embodiments as proposed by the Office Action. The Examiner disagrees, because a reference is no less anticipatory if, after disclosing the invention, the reference then disparages it. The question whether a reference "teaches away" from the invention is inapplicable to an anticipation analysis. *Celeritas Technologies Ltd. v. Rockwell International Corp.*, 150 F.3d 1354, 1361, 47 USPQ2d 1516, 1522-23 (Fed. Cir.1998).

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

The Examiner maintains the rejection.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claims 1-2, 13-18, 20-21, 24, and 26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lethellier (US 6424129).

**Regarding claims 1 and 26:** Lethellier discloses **fig. 1** a load line regulated switched mode power converter for supplying an output voltage and an output current to a load the switched mode power converter comprising:

an inductor a switch **21, 31** coupled to the inductor **23** a first impedance **15** and a power converter (**i.e. fig. 1 and 4**) controller including:

a first sense circuit **15** for obtaining momentary information (**output of 17**) on a first current (**i.e. input current**) flowing through the first impedance **15** the first current (**i.e. input current**) being related to the output current (**i.e. output current flow through 23, 33**),

but does not specifically discloses a second impedance; and means for determining a difference between a zero load voltage and the output voltage to obtain a difference signal, a second sense circuit for obtaining further information on a second current flowing through the second impedance the second current being related to the first current, an integrator for integrating a difference between the further information and the difference signal to obtain a correction signal, and a switch controller for receiving the difference signal the momentary information and the correction signal to control the switch for obtaining a substantially zero correction signal in a steady state.

However in an alternative embodiment **fig. 4**, Lethellier discloses a second impedance **59**; and

means for determining **52** a difference between a zero load voltage (i.e. **reference voltage between 24 and 25**) and the output voltage (i.e. **output voltage**) to obtain a difference signal (**output of 26**) (**Col. 5, lines 40-50**),

a second sense circuit **52** for obtaining further information (**output of 52**) on a second current (**current flow through 59**) flowing through the second impedance **59**,  
an integrator **fig. 2** for integrating a difference between the further information (**output of 52**) and the difference signal (**output of 26**) to obtain a correction signal (**output of fig. 2**), and

a switch controller **27** for receiving the difference signal (**output of 26**) the momentary information (**output of 17**) and the correction signal (**output of fig. 2**) to control the switch **21, 31** for obtaining a substantially zero correction signal in a steady state (**Col. 5 lines 64 through Col 6, lines 1-42 and Col. 7, lines 1-20**).

Therefore, it would have been obvious to one with ordinary skill in the art at the time the invention was made to have modified the first embodiment such as in figure 1 with another embodiment such as in figure 4 as taught by Lethellier in order to have a second sense circuit **52** for obtaining further information (**output of 52**) on a second current (**current flow through 59**) flowing through the second impedance **59** the second current being related to the first current of Lethellier's invention with a reasonable expectation of success because Lethellier teaches an apparatus for

accurately sensing the output current delivered to a load by a buck-type DC-to-DC switched mode power converter that corrects for thermal variation (**Col. 2, lines 43-47**).

**Regarding claim 2:** **fig. 1, and 4** wherein the momentary information has a bandwidth for instantaneously regulating the power converter, and wherein the further information has a further bandwidth lower than the first mentioned bandwidth(**Col. 5 lines 64 through Col 6, lines 1-42 and Col. 7, lines 1-20**).

**Regarding claim 13:** **fig. 1, and 4** wherein the first impedance and the second impedance are the same common resistor and wherein the first current and the second current are the same current.

**Regarding claim 14:** **fig. 1, and 4** wherein the first impedance is an impedance of the main current path of the switch.

**Regarding claim 15:** **fig. 1, and 4** wherein the first impedance is arranged in series with the inductor.

**Regarding claim 16:** **fig. 1, and 4** wherein the second impedance is arranged between an input of the power converter and a main current path of the switch for sensing an average input current of the power converter.

**Regarding claim 17:** **fig. 1, and 4** wherein the power converter is a down-converter comprising a series arrangement of main current paths of the first mentioned switch and a further switch, the inductor being arranged between a junction of the main current paths and an output of the power converter, and wherein the common resistor is arranged in series with the main current path of the first mentioned switch.

**Regarding claim 18:** **fig. 1, and 4** wherein the means for determining the



difference comprises a third resistor arranged between a reference voltage and the output voltage to obtain a difference voltage across the third resistor the difference signal being related to the difference voltage.

**Regarding claim 20: fig. 1, and 4** a switched mode power converter as claimed in claim 1, wherein the power converter is a down-converter comprising a series arrangement of main current paths of the first mentioned switch and a further switch the inductor being arranged between a junction of the main current paths and an output of the power converter, a smoothing capacitor is coupled to a terminal of the main current path of the first mentioned switch directed towards the input of the power converter, and the second impedance is arranged between the input of the power converter and the main current path of the first mentioned switch.

**Regarding claim 21: fig. 1, and 4** wherein the means for determining the difference comprises a third resistor arranged between a reference voltage and the output voltage to obtain a difference voltage across the third resistor the difference signal being related to the difference voltage.

**Regarding claim 24: fig. 1, and 4** an electronics apparatus comprising the switched mode power converter of claim 1.

**Claim 25** rejected under 35 U.S.C. 103(a) as being unpatentable over Lethellier (US 6424129) in view of Bernardon (US 20030214276).

**Regarding claim 25:** Lethellier discloses the limitations of the claim(s) 1 as discussed above, Lethellier the output current of the switched mode power converter of claim 1 being supplied to a load,

but does not specifically disclose a personal computer the output current of the switched mode power converter of claim 1 being supplied to a processor of the personal computer.

Bernardon teaches that a switch mode power converter such as a voltage regulator having the output power provides to an electronic loads such as a computer processors are well know **[paragraph 0004]**.

Therefore, it would have been obvious to one with ordinary skill in the art at the time the invention was made to have modified the switch mode power converter of Lethellier's having the output current supplied to a computer processors as taught by Bernardon invention with a reasonable expectation of success because Bernardon teaches that it is well known to do so.

#### ***Allowable Subject Matter***

Claims 19, 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3-12 allowed.

The following is an examiner's statement of reasons for allowance: As in claim 3, none of the prior art alone or in combination discloses A load line regulated switched

mode power converter for supplying an output voltage and an output current to a load the switched mode power converter including: an inductor a switch coupled to the inductor a first impedance a second impedance and a power converter controller comprising: a first sense circuit for obtaining momentary information on a first current flowing through the first impedance the first current being related to the output current means for determining a difference between a zero load voltage and the output voltage to obtain a difference signal a second sense circuit for obtaining further information on a second current flowing through the second impedance the second current being related to the first current an integrator for integrating a difference between the further information and the difference signal to obtain a correction signal and a switch controller for receiving the difference signal the momentary information and the correction signal to control the switch for obtaining a substantially zero correction signal in a steady state, the switching controller including: a driver for receiving a first driver signal and a second driver signal to operate the switch when a level of the first driver signal reaches a level of the second driver signal, and means for receiving the correction signal for correcting either: (i) the momentary information to obtain corrected momentary information wherein the first driver signal is the corrected momentary information and the second driver signal is the difference signal or (ii) the difference signal to obtain a corrected difference signal wherein the first driver signal is the momentary information (SI) and the second driver signal is the corrected difference signal or (iii) the momentary information to obtain corrected momentary information (CSI) and the difference signal to obtain a

corrected difference signal wherein the first driver signal is the corrected momentary information and the second driver signal is the corrected difference signal.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NGUYEN TRAN whose telephone number is (571)270-1269. The examiner can normally be reached on M-F 7:30-5:00, OFF every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jayprakash N. Gandhi can be reached on 571-272-3740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NT

*/Bao Q. Vu/  
Primary Examiner, Art Unit 2838  
August 24, 2009*